CLAIMS

What is claimed is:

1. A load board interface, comprising:

a plurality of sets of interface nodes, each interface node of each of said plurality of sets of interface nodes configured to connect to corresponding input/output nodes of a semiconductor integrated circuit;

one set of tester nodes, each tester node of said one set of tester nodes configured to connect to one test station of a memory component tester; and

a switching structure

for electrically connecting each tester node of said set of tester nodes to a corresponding one of said interface nodes of each of said sets of interface nodes, and

for electrically connecting at least one interface node of each of said sets of interface nodes to a corresponding one of said tester nodes.

2. A load board interface comprising:

at least one interface circuit comprising:

a set of test nodes configured for electrical coupling with a test station;

a plurality of interface node sets, each set of interface nodes of the plurality being configured for electrical coupling with an individual semiconductor integrated circuit, each set of interface nodes including a plurality of discrete interface nodes wherein each discrete interface node of a set is electrically coupled with a corresponding test node of the set of test nodes, one discrete interface node of each set of the plurality being designated as a compressed output node, and wherein at least one of the compressed output nodes is selectively coupled with the corresponding test node via a switch, the switch being configured to disconnect the at least one compressed output node from the corresponding test node and connect the at least one compressed output node to another test node.

3. The load board interface of claim 2, wherein the at least one set of testing circuitry comprises multiple sets of testing circuitry.

4. The load board interface of claim 2, wherein the at least one compressed output node coupled to the corresponding test node via a switch includes each compressed output node except one, and wherein each compressed output node except one is coupled to the corresponding test node via a mutually independent switch.

5. The load board interface of claim 4, wherein each mutually independent switch is configured to disconnect the compressed output test node associated therewith from the corresponding test node and connect the compressed output test node associated therewith to another test node such that each output test node is connected to a different test node of the set of test nodes.

6. A test system comprising:

a plurality of semiconductor integrated circuits, each of said plurality of semiconductor integrated circuits comprising internal test circuitry for producing at least one compressed test output signal during a first test mode and for producing a plurality of uncompressed test output signals during a second test mode;

at least one test station; and

at least one load board interface having at least one interface circuit comprising:

a set of test nodes electrically coupled with the at least one test station;

a plurality of interface node sets, each set of interface nodes being configured for electrical coupling with an individual semiconductor integrated circuit of the plurality, each set of interface nodes having a plurality of discrete interface nodes wherein each discrete interface node of a set is configured to be electrically coupled with a corresponding test node of the set of test nodes, one discrete interface node of each set being designated as a compressed output node, and wherein at least one of the compressed output nodes is selectively coupled with

the corresponding test node via a switch, the switch being configured to disconnect the at least one compressed output node from the corresponding test node and connect the at least one compressed output node to another test node.

7. A method of testing a plurality of semiconductor integrated circuits, said method comprising:

providing an electrical connection from a plurality of input/output nodes on each of said plurality of semiconductor integrated circuits to a test station;

initiating a first test mode;

receiving a compressed test output signal from each of said plurality of semiconductor integrated circuits at said test station during said first test mode;

determining whether at least one of said plurality of semiconductor integrated circuits is a faulty device during said first test mode; and

if faulty, initiating a second test mode.

8. The method according to claim 7, wherein said initiating a first test mode comprises:

providing input test data to said plurality of input/output nodes on each of said plurality of semiconductor integrated circuits from said test station; and

internally performing a plurality of circuit tests in each of said plurality of semiconductor integrated circuits using said input test data.

9. The method according to claim 8, wherein said internally performing a plurality of circuit tests comprises:

internally generating a plurality of uncompressed test signals in each of said plurality of semiconductor integrated circuits in response to said input test data;

comparing said plurality of uncompressed test signals in each of said semiconductor integrated circuits to determine whether any of said plurality of circuit tests failed; and

internally generating said compressed test output signal in each of said plurality of semiconductor integrated circuits indicative of whether any of said plurality of circuit tests failed.

10. The method according to claim 7, wherein said receiving a compressed test output signal from each of said plurality of semiconductor integrated circuits at said test station comprises:

driving a high impedance to said plurality of input/output nodes on each of said plurality of semiconductor integrated circuits;

driving said compressed test output signal from each of said plurality of semiconductor integrated circuits to one of said plurality of input/output nodes on each of said plurality of semiconductor integrated circuits; and

switching each of said compressed test output signals from said plurality of semiconductor integrated circuits to a distinct input/output pin on said test station.

11. The method according to claim 7, wherein said determining whether at least one of said plurality of semiconductor integrated circuits is a faulty device comprises detecting a high impedance on an input/output pin on said test station corresponding to said compressed test output signal received from said at least one of said plurality of semiconductor integrated circuits.

12. The method according to claim 7, wherein said initiating a second test mode comprises individually testing each said determined faulty device.

13. The method according to claim 12, wherein said individually testing each said determined faulty device comprises:

connecting one said determined faulty device to said test station;

providing input test data to said plurality of input/output nodes on said one determined faulty device from said test station;

internally performing a plurality of circuit tests in said one determined faulty device using said input test data; and

using said test station to determine which of said circuit test is failed.

14. The method according to claim 13, wherein said internally performing a plurality of circuit tests comprises:

internally generating a plurality of uncompressed test signals in said one determined faulty device in response to said input test data; and

outputting each of said plurality of uncompressed test signals to said test station.